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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/765,027

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Kwan Ju Koh

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EXAMINER

NOVACEK, CHRISTY L

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/765,027	<b>Applicant(s)</b> KOH, KWAN JU	
	<b>Examiner</b> Christy L. Novacek	<b>Art Unit</b> 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 26 January 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

This office action is in response to the communication filed January 26, 2004.

#### ***Claim Objections***

Claim 1 is objected to because of the following informalities:

In line 18 of claim 1, "an" should be changed to "a".

Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In line 15 of claim 1, a word such as "layer" or "gate " should be added after "polysilicon".

In line 19 of claim 1, it is unclear as to which of the previously recited nitride layers "the nitride" is referring.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

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having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (US 6,309,933) in view of Yagashita et al. (US 6,607,952).

Regarding claim 1, Li discloses forming a first oxide layer (12) on a surface of an active region of a substrate (10) and implanting ions therein to form a low-doped drain (65) in the active region, forming a nitride layer (22), removing a part of the nitride layer and the oxide layer where a gate will be located and etching the substrate corresponding to the part by a predetermined depth, forming a second oxide layer (32) over an exposed portion of the substrate, implanting ions (38) into the substrate, removing the second oxide layer, depositing a gate insulating layer (40) and a polysilicon layer (42), polishing until the nitride layer is exposed, removing the nitride layer, depositing a conformal oxide layer (62) and a second nitride layer (64), etching the second nitride layer to form a gate sidewall (70) of nitride, implanting ions (72) into the substrate to form a source and drain (68) at both sides of the gate and removing an exposed oxide layer (col. 3, ln. 50 – col. 5, ln. 67). Li does not disclose selectively forming a shallow trench isolation in a substrate. Yagashita discloses forming a shallow trench isolation (12/13) in the substrate of an integrated circuit in order to electrically isolate the active regions on the substrate so that multiple devices may be formed on the substrate, as is well-known in the art (col. 4, ln. 59-62). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form shallow trench isolation regions in the substrate of Li, as shown by Yagashita, because it is conventional in the art to form these regions for the purpose of electrically isolating active regions on an integrated circuit substrate.

Regarding claim 2, Li discloses that the substrate is a silicon substrate (col. 3, ln. 23-25).

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Regarding claim 3, Yagashita discloses that the shallow trench isolation includes oxide layers (col. 4, ln. 59-62).

Regarding claim 4, Li discloses that the predetermined depth is about 800-1200 Angstroms (col. 4, ln. 9-13).

Regarding claim 6, Li discloses that the step of polishing until the nitride layer is exposed, includes a chemical mechanical polishing (CMP) step (col. 4, ln. 45-48).

Regarding claim 7, Li discloses that the second nitride layer is removed by an etch back process (col. 5, ln. 53-55).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. and Yagashita et al. as applied to claim 1 above, and further in view of Bovaird (US 4,830,975).

Regarding claim 5, Li discloses growing the second oxide layer to have a thickness of about 100-150 Angstroms, but Li does not disclose the particular temperature range used to grow the oxide (col. 4, ln. 14-18). Like Li, Bovaird discloses oxidizing a silicon substrate to grow a thin layer of oxide thereon. Bovaird states that this thin oxide layer can be formed by a wet oxidation method at a temperature of 750°C (col. 2, ln. 64-65). At the time of the invention, it would have been obvious to one of ordinary skill in the art to grow the second oxide layer of Li by the oxidation process taught by Bovaird because Li does not disclose any particular temperature to be used and Bovaird teaches that a wet oxidation done at 750°C can successfully oxidize a thin layer of a silicon substrate.

### ***Conclusion***

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The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Nishinohara (US 6,465,842) and Park (US 6,642,130) disclose forming elevated LDD regions for a MOSFET.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN  
March 2, 2005

  
**AMIR ZARABIAN**  
SUPERVISOR/PATENT EXAMINER  
MICROBIOLOGY CENTER